



DIAMOND SYSTEMS CORPORATION

Transition Guide

GPIO-MM

Replacement for GMM-24 and GMM-48

Revision 1.0

June 23, 2006

© Copyright 2006
Diamond Systems Corporation
1225 Terra Bella Ave.
Mountain View, CA 94043
Tel (650) 810-2500
Fax (650) 810-2525
www.diamondsystems.com

Table of Contents

1. INTRODUCTION

This guide is targeted for existing users of the Diamond Systems Corporation Garnet-MM-24 (GMM-24) or Garnet-MM-48 (GMM-48) board, who are, or will be, migrating to the GPIO-MM board.

The GPIO-MM is a superset of the Garnet-MM product line. It combines two Diamond Systems I/O boards, GMM-48 and QMM-10, into a single board. The I/O registers for the GMM portion of GPIO-MM are fully upward compatible with GMM, so software designed for the GMM will work with the GPIO-MM without change. However, before you begin the transition it is a good idea to read this guide and understand all of the differences and new features.

Customers who have not used the Garnet MM before may also be interested in this guide to read what improvements have been made for the GPIO-MM.

It is important to note that all software written for the GMM-24/48 will work on the GPIO-MM without modification. The GPIO-MM I/O register map – the means by which software interacts with the board – is a superset of the GMM-24/48 at power-on. Since the GPIO-MM also provides 10 counter/timers, it offers additional registers not found in the Garnet MM boards.

2. TRANSITION ISSUES

1. Garnet-MM allows the selection, via jumper, of up to two IRQ sources (C0-1, C3-1, C0-2, C3-2). GPIO-MM does not provide for jumper selection of IRQ sources. GPIO-MM defaults to C0-1 as the only interrupt source. Developers must provide software to program the board to accept other IRQ sources.
2. In addition to the 10 counter / timers, the GPIO-MM has other enhanced features that may prove useful in your application. These include 256 bytes of EEPROM storage for configuration data, 16 fixed direction digital I/O lines, and 4 auxiliary I/O lines. Finally, GPIO-MM is based on an FPGA which may be reprogrammed or reconfigured on the board. Thus, GPIO-MM is a highly flexible solution that may serve a variety of embedded application needs.
3. The Garnet MM external connector offers 24 DIO lines and 24 ground pins (See Figure 1 below). There is one connector on the GMM-24 and two connectors on the GMM-48. GPIO-MM combines all 48 digital I/O pins on a single 50 pin connector (See Figure 2 below). The connector is the same type as used on GMM-24 / 48. One row of 25 pins on GPIO-MM matches the active pins on the left connector of GMM-24/48. The second row of 25 pins matches the active pins on the right connector on the GMM-48. Within each row, the pin definition is the same between GPIO and GMM-24/48.

Figure 1. Garnet MM Connectors

J3 (8255#1)			J4 (8255#2 - GMM-48 only)				
A7	1	2	Ground	D7	1	2	Ground
A6	3	4	Ground	D6	3	4	Ground
A5	5	6	Ground	D5	5	6	Ground
A4	7	8	Ground	D4	7	8	Ground
A3	9	10	Ground	D3	9	10	Ground
A2	11	12	Ground	D2	11	12	Ground
A1	13	14	Ground	D1	13	14	Ground
A0	15	16	Ground	D0	15	16	Ground
C7	17	18	Ground	F7	17	18	Ground
C6	19	20	Ground	F6	19	20	Ground
C5	21	22	Ground	F5	21	22	Ground
C4	23	24	Ground	F4	23	24	Ground
C3	25	26	Ground	F3	25	26	Ground
C2	27	28	Ground	F2	27	28	Ground
C1	29	30	Ground	F1	29	30	Ground
C0	31	32	Ground	F0	31	32	Ground
B7	33	34	Ground	E7	33	34	Ground
B6	35	36	Ground	E6	35	36	Ground
B5	37	38	Ground	E5	37	38	Ground
B4	39	40	Ground	E4	39	40	Ground
B3	41	42	Ground	E3	41	42	Ground
B2	43	44	Ground	E2	43	44	Ground
B1	45	46	Ground	E1	45	46	Ground
B0	47	48	Ground	E0	47	48	Ground
+5	49	50	Ground	+5	49	50	Ground

Figure 2. GPIO-MM Connector

J4 (8255#1 and 8255#2)

A7	1	2	D7
A6	3	4	D6
A5	5	6	D5
A4	7	8	D4
A3	9	10	D3
A2	11	12	D2
A1	13	14	D1
A0	15	16	D0
C7	17	18	F6
C6	19	20	F6
C5	21	22	F5
C4	23	24	F4
C3	25	26	F3
C2	27	28	F2
C1	29	30	F1
C0	31	32	F0
B7	33	34	E7
B6	35	36	E6
B5	37	38	E5
B4	39	40	E4
B3	41	42	E3
B2	43	44	E2
B1	45	46	E1
B0	47	48	E0
+5V	49	50	Ground